A SAW-less RF-SoC for cellular IoT Supporting EC-GSM-IoT -121.7 dBm Sensitivity Through EGPRS2A 592 kbps Throughput

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***Abstract*—The latest extended-coverage (EC-GSM-IoT) and high-throughput (EGPRS2A) enhancements make GSM competitive to LTE-based cIoT standards such as NB-IoT with the advantage of global coverage today. This work introduces the first fully-integrated RF-SoC supporting the complete GSM standard family ranging from EC-GSM-IoT through EGPRS2A. The RF-SoC achieves -121.7 dBm receiver sensitivity and peak data rates close to 600 kbps enabling a broad range of IoT applications.**

I. Introduction

With LTE-based 4G smart-phones firmly established globally, the cellular community has begun mapping out the 5th generation of wireless standards, which starts to bifurcate in order to both provide continued support for high throughput smart-phone applications and open up new avenues to Low-Power Wide Area Network (LPWAN) devices deployable at low cost in massive quantities for Machine to Machine (M2M) communication or cellular IoT (cIoT). For the latter path several new standards have been finalized recently, notably LTE Cat-M1 (eMTC), Cat-NB1 (NB-IoT), and Extended-Coverage GSM for the IoT (EC-GSM-IoT), as the cellular industry's answer to competing LPWAN initiatives based on unlicensed spectrum [1]. Coverage extension, up to 20 dB (15 km or 164 dB MCL) beyond legacy sensitivity [2], is a common feature in those standards, which will complement existing PAN/WLAN-based devices to provide rich wireless support to a wide range of potential IoT applications. While there is a palpable excitement about upcoming LTE-based cIoT standards, 60% of existing devices for M2M or cIoT applications are based on legacy GPRS/EGPRS. GSM networks still provide the most extensive global coverage and that is unlikely to change soon, for which EC-GSM-IoT provides an important upgrade path. An option for higher throughput was also standardized (EGPRS2A, 0.6 to 1.2 Mbps) but not taken up enthusiastically so far with only a few exceptions [3], [4]. The cIoT requirements such as those foreseen by LTE Cat-M1 may shed a different light on EGPRS2A if it can be combined with EC-GSM-IoT without much cost penalty. Enhancing the Digital Baseband (DBB) implementation of [3] with RF circuitry and EC-GSM-IoT support, this paper reports the first complete physical layer RF-SoC to support EC-GSM-IoT, legacy GSM, GPRS, and EGPRS, as well as EGPRS2A.

II. EC-GSM-IoT

Extended coverage up to 164 dB MCL poses challenging requirements for EC-GSM-IoT in terms of receiver sensitivity for both timing synchronization and data reception because received signals now drop to well below the thermal noise level (below -6 dB SNR [2]) where conventional GSM synchronization no longer suffices.

A. Timing Synchronization

Traditional GSM synchronization is done in two steps. First, the receiver is turned on and a search for a Frequency Burst (FB), a short sine transporting the Frequency Correction CHannel (FCCH), starts. One hardware efficient FB Detection (FBD) algorithm exploits the statistical properties of the FB [5]. It computes the block-wise variance σ_N of the inter-sample phase difference of the received IQ-samples $\boldsymbol{n}[\cdot]$:

$$\sigma_N = \mathrm{var}\left\{ \bigcup_{i=0}^{N-2} \{\angle \boldsymbol{n}[i] - \angle \boldsymbol{n}[i+1]\} \right\} \tag{1}$$

where N is the block size. Since an FB is a continues stream of GMSK-modulated '1's, σ_N is zero in the absence of noise or a radio channel. The block-wise variance σ_N can be compared against a threshold to decide on an FBD hit. This method gives a coarse estimate of the beginning of the FB with an uncertainty below $\pm N$ symbols. An FBD miss is defined here as not detecting an FB or detecting an FB with a timing-offset error larger than $\pm N$ symbols. The FBD miss rate performance with $N = 16$ and a threshold of 0.05 is depicted in Fig. 1 for an AWGN scenario. After an FB hit, a Synchronization Burst (SB), carrying the Synchronization CHannel (SCH), needs to be detected. The SCH is always transmitted 1 frame after the FCCH. The SB's long training sequence can be used to get a fine-grained time-synchronization estimate $\hat{\eta}$ by means of cross-correlating with a local copy of the training sequence $\boldsymbol{t}[\cdot]$:

$$\hat{\eta} = \arg\max_{\eta} \left\{ \sum_{i=0}^{T-1} \boldsymbol{t}[i] \cdot \boldsymbol{n}^*[\eta + T - i - 1] \right\}, \tag{2}$$

where T is the length of the training sequence and the search space of η must account for the FBD uncertainty.

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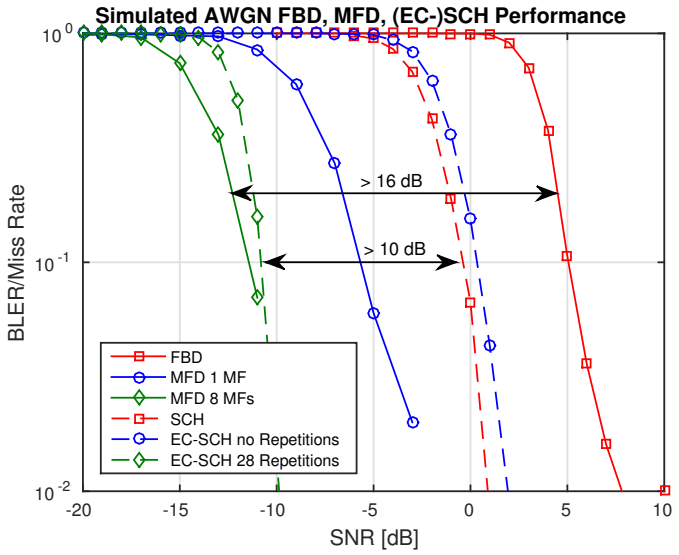

Fig. 1. MFD compared to legacy FBD and EC-SCH compared to legacy SCH performance in an AWGN scenario.

As can be seen from Fig. 1, legacy FBD does not suffice for EC-GSM-IoT and its targeted SNR levels below -6 dB SNR.

To overcome this shortage, in a first step the beginning of a Multi-Frame (MF) needs to be detected which can be done by exploiting the a priori knowledge of the positions of the 5 FCCHs within an MF. An MF Detection (MFD) algorithm has been developed in this work which detects the MF boundary by using multiple FCCHs jointly. It first filters the received samples around the FCCH sine in order to improve the SNR. Then, it computes the block-wise variance σ_N of the inter-sample phase difference of the received samples as in Eq. (1). The σ_N values can get accumulated over multiple MFs for averaging, here the resulting vector of σ_N values is denoted as $\boldsymbol{\sigma}_N[\cdot]$. A Maximum Likelihood (ML) detector estimates the beginning of MF η_{MF}:

$$\hat{\eta}_{MF} = \arg\min_{\eta} \left\{ \sum_{i \in \boldsymbol{F}} \boldsymbol{\sigma}_N[i+\eta] \right\}, \tag{3}$$

where $\boldsymbol{F}$ holds the indices of unbiased FCCH positions. An MFD miss is defined here as detecting the beginning of an MF with a timing offset error larger than $\pm N$ symbols. As can be seen in Fig. 1 for an AWGN scenario with $N = 50$ an MFD miss rate of 10% is achieved at -5 dB SNR or at -11 dB SNR when averaging over 1 and 8 MFs, respectively. This is an improvement of 10 and 16 dB over legacy. In a second step the timing estimation is refined using cross-correlations with the Extended-Coverage SCH (EC-SCH) training sequence as described in Eq. (2).

B. Blind Repetition

The BLER performance of the legacy SCH and Packet Data Traffic CHannel (PDTCH) is improved for the EC-SCH and Extended-Coverage PDTCH (EC-PDTCH) by the use of blind repetitions. While the highest Coverage Class (CC) allows for the transmission of 16 copies for the EC-PDTCH, the EC-SCH consists of 28 repetitions leading to a theoretical gain of 14.4 dB over a single transmission. The potential gain over the legacy SCH is slightly lower due to a higher underlying code-rate (0.38 vs 0.32). Although all of the 28 subsequent transmissions do contain the same information, only groups of seven SBs are exact copies. The four distinct groups differ as the encoded word is shifted cyclically based on the TDMA frame number. This enables the receiver to not only decode the EC-SCH itself, but also detect two bits of the frame number by decoding the received codeword with 4 different cyclic shifts. If we denote the received SBs as $\boldsymbol{b}[\cdot]$, where each index corresponds to one equalized and demapped codeword consisting of Log-Likelihood Ratios (LLRs), the set of codewords S_n which will be decoded after having received n (an integer multiple of 7) SBs is:

$$S_n = \bigcup_{h=0}^{3} \left\{ \sum_{s=0}^{\min\left(\lfloor \frac{n-1}{7} \rfloor, 3\right)} \sum_{i=0}^{6} \boldsymbol{b}\left[n - 7s - i - 1\right]^{(h-s) \bmod 4} \right\}, \tag{4}$$

where the exponent represents the cyclic shift operation and the sum operators are element-wise sums over the SB length.

Simulation results in Fig. 1 of the EC-SCH assuming a perfect timing synchronization show, that a simple Chase-combining scheme that aggregates the LLRs of each repetition after a per-burst channel estimation and equalization achieves 10 dB gain over legacy SCH on an AWGN channel. The limiting factor at very low SNR is the channel estimation. While in general combining unequalized IQ-samples can increase the effective SNR observed during channel estimation, the required phase estimation to remove the existing random phase difference between two EC-SCH repetitions inhibits any gain over Chase-combining at the targeted SNR range. Note, that IQ-combination in fact can improve the decoding performance compared to Chase-combining for the EC-PDTCH. The underlying reason is, that the transmitted EC-PDTCH copies within one frame are phase coherent per standard.

III. EGPRS2A

Although only small data rates are expected at extended reach, many future use cases may arise that also require considerably higher throughput than EC-GSM-IoT or legacy GPRS/EGPRS modules, from a similarly low cost solution. EGPRS2A data rates are significantly larger than targeted in NB-IoT and, in fact, even surpass Cat-M1 data rates within a 200 kHz narrowband. The high spectral efficiency results from a higher modulation order (32-QAM) in the context of inherently high Inter Symbol Interference (ISI) for GSM channels, which pose very tough challenges for the equalizer [3]. Channel shortening filter and reduced-state Soft-Output Viterbi Equalizer (SOVE) are combined to overcome these challenges.

IV. RF-SoC Implementation

Fig. 2 shows a block diagram of the RF-SoC, which consists of an RF transceiver with no need for external SAW filters in either receive or transmit path, and a DBB. The latter is partitioned into three modules supporting control, transmit, and receive. The receive module itself consists of Digital Front End (DFE), DETector (DET), and DECoder (DEC).

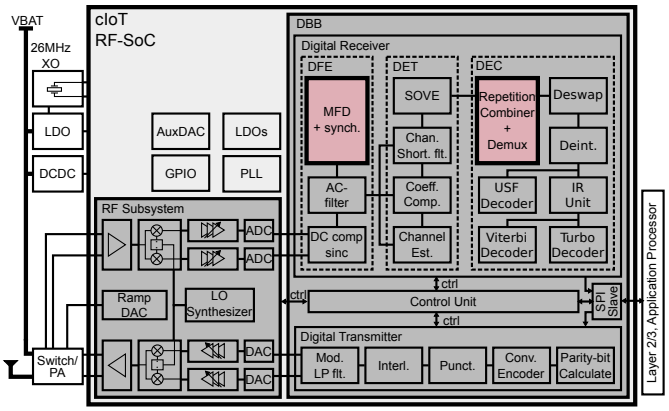

Fig. 2. Block diagram of the EC-GSM-IoT/EGPRS2A RF-SoC. The highlighted blocks (MFD and repetition combination) are depicted in more detail in Fig. 3 and Fig. 4, respectively.

In the present DBB solution multiple FCCHs are detected jointly for MFD in a dedicated VLSI implementation which does not require storing IQ-samples of an entire MF. Fig. 3 illustrates the corresponding digital circuit. It is partitioned into three stages. In the first stage the phases of IQ-samples get calculated using a CORDIC with 12 iterations. The same stage performs the subsequent block-wise computation of σ_N according to Eq. (1), as well. In the second stage the σ_N values get accumulated over multiple MFs and the resulting $\boldsymbol{\sigma}_N[\cdot]$ is stored in the σ-memory. In the third stage an address generation unit loops over $\boldsymbol{F}+\eta$ using the ML detector from Eq. (3) to detect the beginning of MF $\hat{\eta}_{MF}$.

The RF-SoC takes full advantage of repetitive transmissions for the EC-SCH and EC-PDTCH in terms of Chase-combination making it more robust to channel variations as opposed to IQ-combining. The repetition combiner block

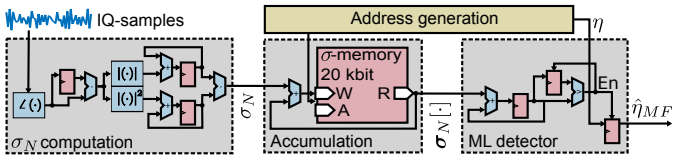

Fig. 3. EC-GSM-IoT MFD circuitry.

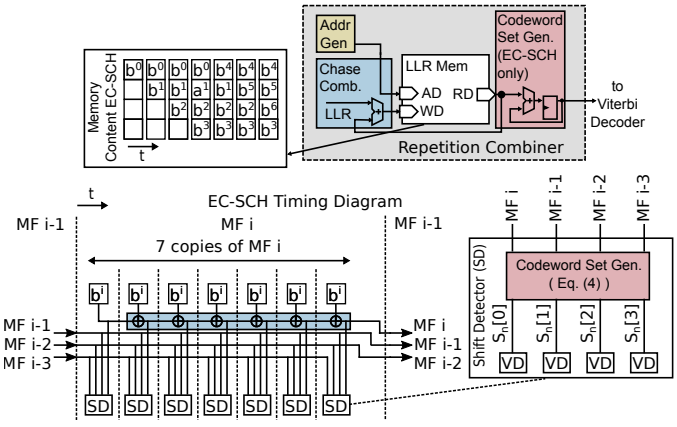

Fig. 4. Repetition combiner circuitry and timing diagram.

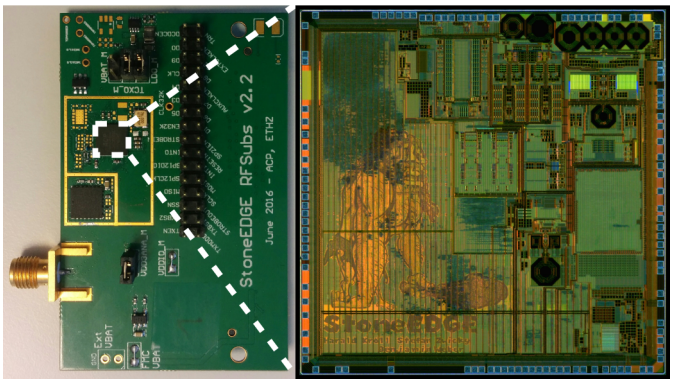

Fig. 5. System PCB (left) and die microphotograph (right).

diagram is depicted in Fig. 4 using a memory hardmacro to hold the intermediate Chase-combined LLRs. Special care is required in case of EC-SCH repetition combining: The decoding attempts of the received copies follow a sliding window approach and four decoding attempts are required to evaluate all four candidates in S_n. A timing diagram for the EC-SCH case for a single MF is illustrated in Fig. 4. Therein, repetitions of a single MF are immediately Chase combined, whereas the inter MF Chase combination is done in a separate codeword-set-generation step resulting in the four codeword candidates $S_n[0]$ to $S_n[3]$ which are evaluated by a Viterbi Decoder (VD). The memory footprint during the reception of 7 subsequent MFs b^0 to b^6 is shown in Fig. 4, as well. As the EC-SCH can occupy 4 MFs at most, storing four blocks of combined LLRs is sufficient with the fifth received MF overwriting the first one. The generation and evaluation of the four codeword candidates is done in a sequential fashion with the inter-MF Chase-combining done on the fly when streaming a codeword candidate to the VD.

The RF-SoC has been implemented in a 130-nm CMOS technology with a chip area of 13.7 mm^2 and is embedded into a 7x7 BGA package. 50% (1.3 MGE) of the core is occupied by the DBB. The DBB has a total of 290 kbit SRAM hardmacros. The DBB operates within 3 clock domains, the 26 MHz GSM clock for control operations and RF interface, a 89 MHz DBB clock for computationally complex units, and an SPI clock domain for layer 2 and 3 communication. A die microphotograph and the system PCB holding the packaged RF-SoC, a commercial PA module with embedded transmit/receive and band-select antenna switches as well as matching networks are depicted in Fig. 5.

V. Measurement Results

The RF-SoC's performance has been measured at the device input considering the required matching network. Fig. 6 shows measured BLER and miss rates for various test cases. In terms of synchronization the 10% miss rate MFD performance when averaging over 8 MFs was measured at -128.5 dBm receive power. The measured 10% BLER sensitivity for EC-SCH is -123.7 dBm. At the EC-GSM-IoT end, -121.7 dBm 20% EC-PDTCH BLER sensitivity has been measured with the EC-MCS1 coding scheme in the highest CC (16 repetitions). An FPGA prototype for an improved version of the present chip which benefits from intra-frame IQ-combining enabled by

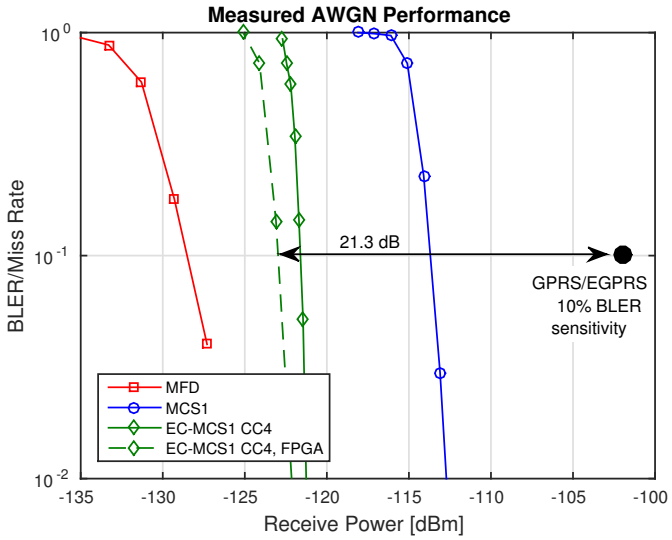

Fig. 6. Measured EC-GSM-IoT performance.

EC-PDTCH phase coherency shows −123.3 dBm (> 164 dB MCL) is achievable. This is highly competitive compared with the anticipated NB-IoT sensitivity. Legacy GPRS CS1 and legacy EGPRS MCS1 coding schemes achieve a 10%-BLER sensitivity of −113.3 dBm and −113.7 dBm, respectively, which are already 11.3 dB and 11.7 dB better than the requirements specified by 3GPP. Hence, EC-GSM-IoT gives an additional gain of 8 dB for the present implementation and 9.6 dB for the improved version.

Measured throughput vs received signal power at the device input is plotted in Fig. 7 showing that the RF-SoC enables to trade-off throughput vs sensitivity for a receive-power range as large as 40 dB. With EC-GSM-IoT the RF-SoC still achieves 1 kbps throughput for very low signal levels. At the EGPRS2A end, a maximum throughput of 592 kbps has been demonstrated in the supported multislot class 45.

The overall performance of the RF-SoC is summarized

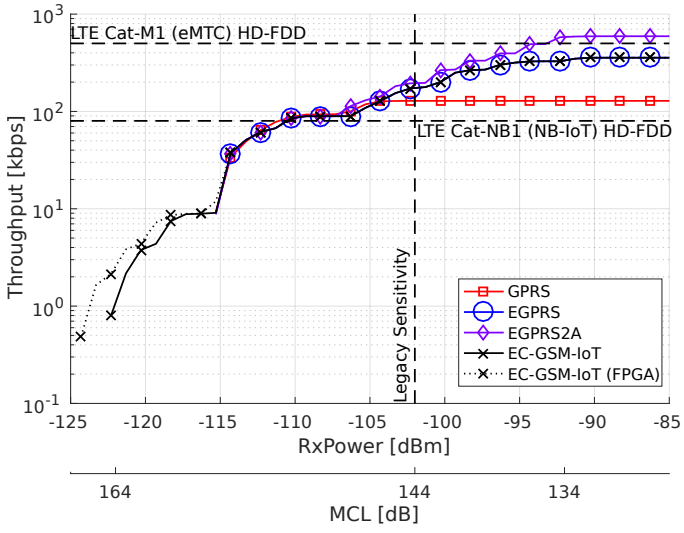

Fig. 7. Measured throughput vs receive power or MCL for the present RF-SoC compared to competing cIoT standards.

TABLE I. COMPARISON TO PRIOR-ART SOLUTIONS FOR THE E-GSM-900 BAND UNDER AWGN CHANNEL CONDITIONS.

Parameter	This work	[7]	[6]	[4][2]
EC-GSM-IoT sensitivity [dBm]	-121.7	n/a[3]	n/a[3]	n/a[3]
EC-GSM-IoT power [mW]	156.6[1]	n/a[3]	n/a[3]	n/a[3]
EGPRS2A throughput [kbps]	592.2	n/a[3]	n/a[3]	493.5
EGPRS throughput [kbps]	356.4	n/a[4]	297	297
GPRS throughput [kbps]	128.4	n/a[4]	107	107
Supported multislot class	45	n/a[4]	33	33
RBER II sensitivity [dBm]	-110.5	-110.3	-110	n/a[4]
SAW-less	yes	yes	no	n/a[2]
Technology [nm]	130	65	65	28

[1] complete RF-SoC averaged over one receive EC-MCS1 CC4 TTI
[2] DBB only, separate RF transceiver chip required
[3] not supported
[4] not provided

in Table I and compared to prior-art solutions [4], [6], [7]. Only this RF-SoC supports EC-GSM-IoT, EGPRS2A, and the highest multislot class 45 together which leads to a coverage increase of more than 10 dB and at least 20% more throughput compared to the prior-art, but up to 100% compared to non-EGPRS2A solution [6]. The RBER II sensitivity is comparable to the prior-art solutions.

VI. CONCLUSION

An RF-SoC has been presented with support for EC-GSM-IoT, GSM, GPRS, EGPRS, and EGPRS2A enabling a BLER sensitivity of -121.7 dBm and a throughput of 592 kbps. As the aspirations for cIoT, with extended coverage, enjoy a warm embrace by three recent cellular standards (EC-GSM-IoT, Cat-M1, NB-IoT), this RF-SoC adds to that enthusiasm as well as sense of urgency by leading the realization for the GSM path.

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